WHAT IS CLAIMED IS:

1. A scalable data processing system, including:

a first set of central processing units;

a first system memory accessible to the first set of processors;

scalability logic to connect the data processing system to a second data processing system, having a second set of processors and a second system memory, to form a scaled system;

a set of scalability ports connected to the scalability logic to receive scalability cables connecting the first system to the second system; and

system management to cause each of the system's scalability ports to issue an identifiable signal and further configured to detect the reception of an identifiable signal, sent by another system, by any of the scalability ports and to report the reception of the signal to a system management of the second system to determine which ports of the two systems are connected by the cable.

2. The system of claim 1, wherein the system management includes a service processor connected to the system via an adapter card and wherein the service processor is connected to a service processor of other systems via a network medium.

3. The system of claim 1, wherein the system management causes a scalability port to issue an identifiable signal by causing the assertion of a bit in a register corresponding to the set of scalability ports.

4. The system of claim 3, wherein the scalability port register is implemented in a programmable logic device.

5. The system of claim 1, wherein the system management further includes controller logic connected to the service processor via a dedicated serial connection and connected to the programmable logic device via an I2C bus.

6. The system of claim 1, wherein the system management includes means for determining a timeout condition following assertion of a bit, and identifying the corresponding scalability port open.

7. The system of claim 1, wherein the system management further includes code means for using the scalability information to generate a graphical image of scalability interconections.

8. A method of determining scalability cabling between at least two scalable data processing systems, comprising:

driving an identifiable signal on a first scalability port of a first system;

responsive to receiving the identifiable signal by a second system, determining which scalability port of the second system received the distinctive signal;

informing the first system of the reception of the distinctive signal by the determined scalability port of the second system and recording the first scalability port of the first system and the scalability port of the second system as being connected by a scalability cable.

9. The method of claim 8, further comprising detecting a timeout by the first system and, responsive thereto, identifying the first scalability port as being unconnected.

10. The method of claim 8, further comprising, iterating the sequence of claim 8, until all scalability ports have been accounted for.

11. The method of claim 10, further comprising generating a graphical image of the scalability cable connections.

12. The method of claim 8, wherein driving the signal on the first scalability port comprises setting a bit in a register associated with the set of scalability ports.

13. The method of claim 8, wherein setting a bit in the register comprises a controller writing to a specified address on an I2C bus connecting the controller to the register.

14. The method of claim 8, wherein determining the scalability port that received the signal includes reading the bits in a register associated with scalability port.

15. A computer program product comprising computer executable instructions, stored on a computer readable medium, for determining scalability cabling between at least two scalable data processing systems, comprising:

computer code means for driving an identifiable signal on a first scalability port of a first system;

responsive to receiving the identifiable signal by a second system, computer code means for determining which scalability port of the second system received the distinctive signal;

computer code means for informing the first system of the reception of the distinctive signal by the determined scalability port of the second system and recording the first scalability port of the first system and the scalability port of the second system as being connected by a scalability cable.

16. The computer program product of claim 15, further comprising code means for detecting a timeout by the first system and, responsive thereto, identifying the first scalability port as being unconnected.

17. The computer program product of claim 15, further comprising, code means for iterating the sequence of claim 15, until all scalability ports have been accounted for.

18. The computer program product of claim 19, further comprising code means for generating a graphical image of the scalability cable connections.

19. The computer program product of claim 15, wherein the code means for driving the signal on the first scalability port comprises code means for setting a bit in a register associated with the set of scalability ports.

20. The computer program product of claim 15, wherein code means for setting a bit in the register comprises a controller writing to a specified address on an I2C bus connecting the controller to the register.

21. The computer program product of claim 15, wherein the code means for determining the scalability port that received the signal includes code means for reading the bits in a register associated with scalability port.